CLAIMS

I claim:

5   1.   A method comprising:
       receiving a single hardware I/O control block
by a host adapter integrated circuit wherein said
host adapter integrated circuit interfaces two I/O
buses and further wherein said single hardware I/O
10   control block specifies a write data transaction
for a first data storage device; and
       analyzing said single hardware I/O control
block by said host adapter integrated circuit to
determine whether information in said single
15   hardware I/O control block specifies a mirrored
write data transaction for a second data storage
device.

       2.   The method of Claim 1 wherein said analyzing
20   said single hardware I/O control block further
comprises:
       determining, by said host adapter integrated
circuit, whether an entry in a first mirror
hardware I/O control block field of said single
25   hardware I/O control block is valid.

       3.   The method of Claim 2 further comprising:
       generating, by said host adapter integrated
circuit, a second hardware I/O control block upon
30   determining said entry in said first mirror
hardware I/O control block field is valid wherein
said second hardware I/O control block specifies
said mirrored write data transaction for said
second data storage device.

35

       4.   The method of Claim 3 further comprising:

-23-

executing said first hardware I/O control block and said second hardware I/O control block independently by said host adapter integrated circuit.

5

5.   The method of Claim 4 further comprising:
    posting as complete only a last of said first and second hardware I/O control blocks to complete executing.

10

6.   The method of Claim 2 further comprising:
    executing said first hardware I/O control block by said host adapter integrated circuit as a non-mirrored write data transaction upon

15   determining said entry in said first mirror hardware I/O control block field is invalid.

7.   A method comprising:
    receiving a single hardware I/O control block

20 by a host adapter integrated circuit wherein said single hardware I/O control block specifies a write data operation for a first data storage device and includes a sister hardware I/O control block field; and

25   generating another hardware I/O control block by said host adapter integrated circuit upon said sister hardware I/O control block field containing a valid hardware I/O control block identification number wherein said another hardware I/O control

30   block specifies said write data operation for a second data storage device so that said write data transaction is mirrored.

8.   The method of Claim 7 wherein said valid

35 hardware I/O control block identification number is a

pointer to a storage site in an array of hardware I/O control block storage sites.

9. The method of Claim 7 further comprising:
    placing a hardware I/O control block identification number of said single hardware I/O control block in a sister hardware I/O control block field of said another hardware I/O control block.

10. The method of Claim 7 wherein said another hardware I/O control block includes a sister hardware I/O control block field, and said method further comprises:
    placing a null hardware I/O control block identification number in said sister hardware I/O control block field of said single hardware I/O control block upon completion of execution of said another hardware I/O control block prior to completion of execution of said single hardware I/O control block.

11. The method of Claim 7 wherein said another hardware I/O control block includes a sister hardware I/O control block field, and said method further comprises:
    placing a null hardware I/O control block identification number in said sister hardware I/O control block field of said another hardware I/O control block upon completion of execution of said single hardware I/O control block prior to completion of execution of said another hardware I/O control block.

12. The method of Claim 7 further comprising:

reporting completion of execution of only one
of said single hardware I/O control block and said
another hardware I/O control block.

13. The method of Claim 7 further comprising:
reporting completion of execution of said
single hardware I/O control block only if said
sister hardware I/O control block field of said
single hardware I/O control block contains a
predefined value.

14. The method of Claim 7 further comprising:
reporting completion of execution of said
another hardware I/O control block only if said
sister hardware I/O control block field of said
another hardware I/O control block contains a
predefined value.

15. A method comprising:
receiving a single hardware I/O control block
by a host adapter integrated circuit wherein said
single hardware I/O control block specifies a
write data operation for a first data storage
device and includes a sister hardware I/O control
block field;
generating another hardware I/O control block
by said host adapter integrated circuit upon said
sister hardware I/O control block field containing
a valid hardware I/O control block identification
number wherein said another hardware I/O control
block specifies said write data operation for a
second data storage device so that said write data
transaction is mirrored;
placing a hardware I/O control block
identification number of said single hardware I/O
control block in a sister hardware I/O control

block field of said another hardware I/O control block;

placing a null hardware I/O control block identification number in said sister hardware I/O control block field of one of said single hardware I/O control block and another hardware I/O control block upon completion of execution of a different one of said single hardware I/O control block and said another hardware I/O control block wherein said different one is a first to complete execution; and

reporting completion of execution of only one of said single hardware I/O control block and said another hardware I/O control block.

16.   A structure comprising:

a memory containing processor instructions for a host adapter mirroring process, wherein upon execution of said processor instructions said host adapter mirroring process comprises:

receiving a single hardware I/O control block by a host adapter integrated circuit wherein said host adapter integrated circuit interfaces two I/O buses and further wherein said single hardware I/O control block specifies a write data transaction for a first data storage device; and

analyzing said single hardware I/O control block by said host adapter integrated circuit to determine whether information in said single hardware I/O control block specifies a mirrored write data transaction for a second data storage device.

17.   A structure comprising:

a memory containing processor instructions for a host adapter mirroring process, wherein upon execution of said processor instructions said host adapter mirroring process comprises:

5   receiving a single hardware I/O control block by a host adapter integrated circuit wherein said single hardware I/O control block specifies a write data operation for a first data storage device and includes a

10   sister hardware I/O control block field; and generating another hardware I/O control block by said host adapter integrated circuit upon said sister hardware I/O control block field containing a valid hardware I/O control

15   block identification number wherein said another hardware I/O control block specifies said write data operation for a second data storage device so that said write data transaction is mirrored.

20

18. A hardware I/O control block structure stored in a memory, said hardware I/O control block structure comprising:

     a sister hardware I/O control block field; and

25   a target identification field.

19. The hardware I/O control block structure stored in a memory as in Claim 18 wherein said hardware I/O control block structure is one of a plurality of

30 hardware I/O control block structures in said memory.

20. A hardware I/O control block memory array comprising:

     a first hardware I/O control block having a

35   sister hardware I/O control block field; and

a second hardware I/O control block having a sister hardware I/O control block field wherein said sister hardware I/O control block field of said first hardware I/O control block includes a

5   pointer to said second hardware I/O control block and said sister hardware I/O control block field of said second hardware I/O control block includes a pointer to said first hardware I/O control block.

10

21.   A method comprising:

using, in a host system, a single hardware I/O command block structure for both non-mirrored and mirrored transactions for a plurality of

15   storage devices coupled to said host system by a host adapter;

setting a mirror field in said single hardware I/O command block structure to a valid value for a mirrored transaction; and

20   setting said mirror field in said single hardware I/O command block structure to an invalid value for a non-mirrored transaction.

25